REMARKS

Applicant respectfully requests reconsideration of this application, as amended, and consideration of the following remarks.

Office action Rejection Summary

Claims 1-13 and 15-32 were rejected under the first paragraph of 35 U.S.C. § 112, first paragraph.

Claim 14 has been rejected under 35 U.S.C. §103 (a) as being unpatentable over U.S. Patent No. 5,751,710 to Crowther et al. ("Crowther").

Status of Application

Claims 1-32 remain in the application. Claims 14 and 24 have been amended to correct typographical errors. Claims 33-36 have been added. No new matter has been added.

Claims Rejections

Claim 1 has been rejected under the first paragraph of 35 U.S.C. § 112. Applicants respectfully submit that claim 1 contains subject matter that is sufficiently described in the specification to enable those skilled in the art to make and use the claimed subject matter.

Claim 1 recites:

> 1. A method for cell replication comprising:
> receiving a request for data transmission through a crossbar and a corresponding mapping information, the mapping information received by the crossbar and received from one of a plurality of software configurable slot remap registers, the mapping information indicative of a destination slot and a backup destination slot to which the data is to be transmitted; and
> replicating the data by transmitting the data to the destination slot and to the backup destination slot when the data arrives at an input slot of the crossbar.

The Office Action states:

> The term "slot remap register" is not commonly used in the art. Page 8 of the specification merely teaches that the slot remap registers are programmed into the switch planes, and that the resulting replication feature differs from the prior art because it allows implementation through software rather than through hardware. Figure 5 is only a table, and the specification does not teach how to

> make the table, where or how to store it, or how to use it. Figure 4 simply depicts the slot remap register as adjacent squares. Mapping information, the manner of creation of which is left untaught, is delivered to both the Spatial Crossbar 213 and the Logic Scheduler 215. This raises the issue that in order to teach how to make and use the slot remap registers it is necessary to also teach how to make and use the Logic Schedulers. Figure 4 simply depicts the Logic Scheduler as a square, and the specification fails to provide adequate instruction in the manner of making and using the Logic Scheduler. The specification therefore fails to enable one of ordinary skill in the art to make or use the invention as claimed. (Office Action 02/26/02).

Applicants respectfully disagree with the Examiner's characterization of claim 1 and submits that the phrase "slot remap" is sufficiently clear and definite to one having ordinary skill in the art, and that one having ordinary skill in the art would understand this phrase and know, with certainty, what is meant thereby. The slot remap registers are described in detail on page 10, line 10 through page 11, line 4 and again in figure 5 of the application. In particular, the specification states that:

> Figure 5 illustrates exemplary slot remap registers. In the illustrated embodiment, there are fourteen registers with five bits and the most significant bit, bit four, determines whether the corresponding traffic is to go to two slots (i.e., "redundant mode"). The four lower bits determine the identity of the current backup slot (i.e., "remap value"). Each register of the slot remap registers $416_1 \ldots 416_N$ may correspond with one slot (one-to-one correspondence with 14 registers and 14 slots). The backup slot is assigned to 1 to N slots. (Page 10, lines 10-17).

Applicants therefore submit that it is described that each register consists of five bits wherein the last bit (designated as bit number four) is the most significant and is the determining bit in whether traffic is to go to two slots (page 10, lines 11-14). The remaining four bits (labeled 0 through 3) determine the identity of the backup slot (i.e. "remap value") (Fig. 5 and page 10, lines 13-14).

Page 5, line 11 of the application defines, for one embodiment, the term "slot remap" register as a "switch fabric" register. Applicants respectfully note that the phrase "switch fabric" appears in several issued U.S. patents, including number 6,351,454 to Crocker et al. Additionally, the term "switch fabric" appears in the Cisco 12012 Gigabit Switch Router Installation and Configuration Guide publication, Copyright 1997, also available on the "Documentation" website for Cisco Systems, Inc., http://www.cisco.com/univercd/cc/td/doc/product/core/cis12000/cis12012/fru/4343swfc.htm#xtocid227783, 2/29/2001.

Furthermore, in paragraph two of the Office action, the Examiner states that "Figure 4 simply depicts the slot remap registers as adjacent squares." Applicants respectfully disagree with the Examiner's characterization of the slot remap registers. In the description of Figure 4 on page 8, line 21 through page 10, line 9, the switch plane is described in detail, including the slot remap registers, designated 416_1-416_N. Specifically, lines 11 and 12 on page 9 detail that both the crossbar 213 and the scheduler 215 receive mapping information 422 from software configurable slot remap registers 416_1-416_N. As previously stated, the slot remap registers are fully described on page 10, line 10 through page 11, line 4 and again in figure 5 of the application.

Additionally, Applicants respectfully disagree with the Office Action's conclusion that "the specification fails to provide adequate instruction in the manner and making and using the Logic Scheduler." Applicants wish to point out that claim 1 does not recite "Logic Scheduler," but rather "a scheduler." Applicants respectfully submit that "a scheduler" is described in detail on page 8, line 25 through page 10, line 5. Specifically:

> The scheduler's function is described on page 8, line 25 ("a scheduler 215 that controls the crossbar 213.") and page 9, lines 8-10 ("Only data for which a request for transmission is granted by the scheduler 215 is processed through the crossbar 213."); it's inputs, outputs and function of the inputs and outputs are described on page 9, lines 1-5 ("For one embodiment, the scheduler 215 has N signal inputs $408_1 \ldots 408_N$ and N signal outputs $410_1 \ldots 410_N$ and provides control signals $406_1 \ldots 406_N$ to the crossbar 213. The signal inputs $408_1 \ldots 408_N$ to the scheduler 215 are requests for data transmission through the crossbar 213, and the signal outputs $410_1 \ldots 410_N$ are grants (i.e. acknowledgements to the requests)."); it's interrelation with the slot remap registers and input format is described on page 9, lines 11-14 ("Both the crossbar 213 and the scheduler 215 receive mapping information 422 from software configurable slot remap registers $416_1 \ldots 416_N$. Mapping information 422 identifies the data out destination slots $414_1 \ldots 414_N$ to which data is to be transmitted through the crossbar 213."); and a detailed explanation of its manner of use is described on page 9, line 18 through page 10, line 5 ("When a request comes in to, for example, input slot 408_1 of the scheduler 215, the scheduler 215 receives the corresponding mapping information 422 from the slot remap register 416_1. The scheduler 215 then determines whether the destination slot and the backup destination slot as identified by the mapping information 422 for input slot 408_1 are valid based on the result of arbitration (i.e., whether the destination slot and the backup destination slot are available). For example, the scheduler 215 may grant requests based on some type of priority

scheme whereby a grant with the highest predetermined priority is granted a request first and so on. The form of arbitration to select which destination slot to grant next may vary and is not limited to a priority scheme based arbitration. Once validity is confirmed, the scheduler 215 transmits a control signal 406 to the crossbar 213 which indicates that 412_1 is permitted to send a cell to its intended destination slot and the backup destination slot."

For the aforementioned reasons, applicants respectfully submit that claim 1 contains subject matter that is sufficiently described in the specification to enable those skilled in the art to make and use the claimed subject matter.

Given that claims 2-4 depend from claim 1, applicants also submit that claims 2-4 are also patentable.

Each of claims 5, 15, and 24 have been rejected under the first paragraph of 35 U.S.C. § 112. Applicants respectfully submit that claims 5, 15, and 24 contain subject matter that is sufficiently described in the specification to enable those skilled in the art to make and use the claimed subject matter.

Claims 5, 15, and 24 recite:

"data traffic...processed...to a destination slot and to a backup destination slot *according to software configurable mapping information*."
(emphasis added)

The Office Action states:

Claims 5, 15, and 24 specify "according to software configurable mapping information." According to the specification, this "software configurable mapping information" is the "slot remap registers." The term "slot remap register" is not commonly used in the art. Page 8 of the specification merely teaches that the slot remap registers are programmed into the switch planes, and that the resulting replication feature differs from the prior art because it allows implementation through software rather than through hardware. Figure 5 is only a table, and the specification does not teach how to make the table, where or how to store it, or how to use it. Figure 4 simply depicts the slot remap register as adjacent squares. Mapping information, the manner of creation of which is left untaught, is delivered to both the Spatial Crossbar 213 and the Logic Scheduler 215. This raises the issue that in order to teach how to make and use the slot remap registers it is necessary to also teach how to make and use the Logic Schedulers. Figure 4 simply depicts the Logic Scheduler as a square, and the specification fails to provide adequate instruction in the manner of making and

using the Logic Scheduler. The specification therefore fails to enable one of ordinary skill in the art to make or use the invention as claimed. (Office Action 02/26/02).

Applicants respectfully disagree with the Examiner's characterization of claim 5, 15, and 24. Applicants respectfully submit that the phrase "slot remap" is sufficiently clear and definite to one having ordinary skill in the art, and that one having ordinary skill in the art would understand this phrase and know, with certainty, what is meant thereby. The slot remap registers are described in detail on page 10, line 10 through page 11, line 4 and again in figure 5 of the application.

In particular, the specification states that:

> Figure 5 illustrates exemplary slot remap registers. In the illustrated embodiment, there are fourteen registers with five bits and the most significant bit, bit four, determines whether the corresponding traffic is to go to two slots (i.e., "redundant mode"). The four lower bits determine the identity of the current backup slot (i.e., "remap value"). Each register of the slot remap registers $416_1 \ldots 416_N$ may correspond with one slot (one-to-one correspondence with 14 registers and 14 slots). The backup slot is assigned to 1 to N slots. (Page 10, lines 10-17).

Applicants therefore submit that it is described that each register consists of five bits wherein the last bit (designated as bit number four) is the most significant and is the determining bit in whether traffic is to go to two slots (page 10, lines 11-14). The remaining four bits (labeled 0 through 3) determine the identity of the backup slot (i.e. "remap value") (Fig. 5 and page 10, lines 13-14).

Page 5, line 11 of the application defines, for one embodiment, the term "slot remap" register as referring to a "switch fabric" register. Applicants respectfully note that the phrase "switch fabric" appears in several issued U.S. patents, including number 6,351,454 to Crocker et al. Additionally, the term "switch fabric" appears in the Cisco 12012 Gigabit Switch Router Installation and Configuration Guide publication, Copyright 1997, also available on the "Documentation" website for Cisco Systems, Inc., http://www.cisco.com/univercd/cc/td/doc/product/core/cis12000/cis12012/fru/4343swfc.htm#xtocid227783, 2/29/2001.

Furthermore, in paragraph three of the Office action, the Examiner states that "Figure 4 simply depicts the slot remap registers as adjacent squares." Applicants respectfully disagree

with the Examiner's characterization of the slot remap registers. In the description of Figure 4 on page 8, line 21 through page 10, line 9, the switch plane is described in detail, including the slot remap registers, designated 416_1-416_N. Specifically, lines 11 and 12 on page 9 detail that both the crossbar 213 and the scheduler 215 receive mapping information 422 from software configurable slot remap registers 416_1-416_N. As previously stated, the slot remap registers are fully described on page 10, line 10 through page 11, line 4 and again in figure 5 of the application.

Additionally, Applicants respectfully disagree with the Office Action's conclusion that "the specification fails to provide adequate instruction in the manner and making and using the Logic Scheduler." First, Applicants wish to point out that claims 5, 15, and 24 do not recite "Logic Scheduler," but rather "a scheduler." Applicants respectfully submit that the "scheduler" is described in detail on page 8, line 25 through page 10, line 5. Specifically:

> the scheduler's function is described on page 8, line 25 ("a scheduler 215 that controls the crossbar 213.") and page 9, lines 8-10 ("Only data for which a request for transmission is granted by the scheduler 215 is processed through the crossbar 213."); it's inputs, outputs and function of the inputs and outputs are described on page 9, lines 1-5 ("For one embodiment, the scheduler 215 has N signal inputs $408_1 \ldots 408_N$ and N signal outputs $410_1 \ldots 410_N$ and provides control signals $406_1 \ldots 406_N$ to the crossbar 213. The signal inputs $408_1 \ldots 408_N$ to the scheduler 215 are requests for data transmission through the crossbar 213, and the signal outputs $410_1 \ldots 410_N$ are grants (i.e. acknowledgements to the requests)."); it's interrelation with the slot remap registers and input format is described on page 9, lines 11-14 ("Both the crossbar 213 and the scheduler 215 receive mapping information 422 from software configurable slot remap registers $416_1 \ldots 416_N$. Mapping information 422 identifies the data out destination slots $414_1 \ldots 414_N$ to which data is to be transmitted through the crossbar 213."); and a detailed explanation of its manner of use is described on page 9, line 18 through page 10, line 5 ("When a request comes in to, for example, input slot 408_1 of the scheduler 215, the scheduler 215 receives the corresponding mapping information 422 from the slot remap register 416_1. The scheduler 215 then determines whether the destination slot and the backup destination slot as identified by the mapping information 422 for input slot 408_1 are valid based on the result of arbitration (i.e., whether the destination slot and the backup destination slot are available). For example, the scheduler 215 may grant requests based on some type of priority scheme whereby a grant with the highest predetermined priority is granted a request first and so on. The form of arbitration to select which destination slot to grant next may vary and is not limited to a priority scheme based arbitration. Once

validity is confirmed, the scheduler 215 transmits a control signal 406 to the crossbar 213 which indicates that 412_1 is permitted to send a cell to its intended destination slot and the backup destination slot."

For the aforementioned reasons, applicants respectfully submit that claims 5, 15, and 24 contain subject matter that is sufficiently described in the specification to enable those skilled in the art to make and use the claimed subject matter.

Given that claims 6-13 depend from claim 5, claims 16-23 depend from claim 15, and claims 25-32 depend from claim 24, applicants submit that claims 6-13, 16-23, and 25-32 are also patentable.

Rejections under 35 U.S.C. § 103

Claim 14 has been rejected under 35 U.S.C. § 103(a) as being obvious over Crowther et al. in view of the admitted prior art. Applicants respectfully submit that claim 14 is patentable over the cited references.

Amended claim 14 recites:

> 14. A network switch system comprising:
> a plurality of processor cards comprising a central processing unit and high level software;
> a plurality of switch cards coupled to the plurality of processor cards and *implemented with a cell replication feature*, the plurality of switch cards comprised of a plurality of switch planes; and
> a plurality of line cards coupled to the plurality of switch cards, the plurality of line cards to interface the plurality of switch cards with traffic coming in and out of a plurality of physical ports.
> (Emphasis added)

Applicant respectfully disagrees with the Office Action's conclusion. Maximum data rates are achieved in Crowther by interconnecting network cards through a mesh backplane comprising direct and indirect paths between the cards and thereafter transferring the data over those paths. Crowther does not teach or suggest a network switch system with a cell replication feature.

Applicants believe the Examiner to be in agreement with such characterization of Crowther. In particular, the Office Action states: "Crowther et al. fails to teach that the switch cards perform cell replication." (Office Action, 2/26/02).

Furthermore, the background of the present application discusses prior art with APS implemented electrically through a multiplexer (MUX)/combination on a line card. Applicants believe the Examiner to be in agreement with such characterization of the admitted prior art. In particular, the Office Action states: "The Admitted Prior Art teaches a line card comprising a multiplexer/buffer combination, which is used to replicate cells." (Office Action, 2/26/02). The cited references do not teach cell replication through switch cards of a network switch using high-level software to channel data traffic through a plurality of physical ports. As such, Crowther, either alone or in combination with Applicant's Admitted Prior Art fails to teach or suggest a plurality of switch cards implemented with a cell replication feature.

In contrast, claim 14 recites a network switch comprised of a central processing unit and high-level software controlling a plurality of switch cards implemented with a cell replication feature with a plurality of line cards interfacing traffic coming in and out of a plurality of physical ports with the switch cards. Therefore, applicant respectfully submits that claim 14 is patentable over the cited references.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

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Dated: 7/3, 2002

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CLAIMS

VERSION WITH MARKINGS TO SHOW CHANGES

14. (Amended) A network switch system comprising:

a plurality of processor cards comprising a central processing unit and high level software;

a plurality of switch cards coupled to the plurality of processor cards and implemented with a cell replication feature, the plurality of switch cards [comprises] comprised of a plurality of switch planes; and

a plurality of line cards coupled to the plurality of switch cards, the plurality of line cards to interface the plurality of switch cards with traffic coming in and out of a plurality of physical ports.

24. (Amended) An apparatus for cell replication comprising:

[mean] means for directing data traffic; and

means for controlling the means for directing, the means for controlling coupled to the means for directing comprising a plurality of signal inputs and a plurality of signal outputs and configured to provide control signals to the means for directing, the plurality of signal inputs being requests for data transmission through the means for directing, and the plurality of signal outputs being grants to the requests, data for which a request for transmission is granted by the means for controlling is replicated and processed through the means for directing to a destination slot and to a backup destination slot according to software configurable mapping information.

Claims 33-36 have been added.